

Design and Experimental Validation of a Safe Control Strategy for Reconfigurable Batteries

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Abstract—In this paper, we present a novel control strategy for optimizing the management of reconfigurable batteries, particularly in electric vehicles (EVs) and energy storage systems. Our approach uniquely integrates Control Allocation (CA) with Control Barrier Functions (CBF) to enhance operational efficiency while enforcing electro-thermal safety constraints. Specifically, the proposed control scheme regulates the output voltage and ensures State-of-Charge (SoC) balancing across battery modules, addressing the common weakest-module problem. Additionally, it dynamically adjusts power distribution to provide over-temperature protection, mitigating the risk of thermal runaway. Our feasibility analysis establishes the conditions under which the CBF-based safety constraints are satisfied, ensuring the existence of feasible control actions. Furthermore, we define comprehensive performance metrics to evaluate and compare the controller’s effectiveness. This includes CBF gain tuning based on feasibility results. We perform scalability analysis, demonstrating the controller’s effectiveness in systems with a large number of modules, which is critical for EV applications where computational efficiency is paramount. Finally, experimental validation on a small-scale prototype showcases the practical capability of our CBF-based optimal controller.

Index Terms—Reconfigurable Batteries, Control Barrier Functions, Control Allocation, SoC Balancing, Electro-Thermal Safety Constraints

I. INTRODUCTION

Battery Electric Vehicles (BEVs) have the potential to significantly reduce environmental impacts and improve air quality compared to conventional gasoline-powered vehicles [1, 2]. BEVs produce zero tailpipe emissions and lower overall lifecycle greenhouse gas emissions. [3] Recognizing these advantages, many countries have established ambitious targets for Electric Vehicle (EV) adoption, with several nations planning to phase out sales of new gasoline-powered vehicles between 2030 and 2040 [3, 4].

Battery Management Systems (BMSs) are critical to ensuring the safety, reliability, and performance of battery packs [5, 6]. BMSs are responsible for performing a wide range of key functions, including State-of-Charge (SoC) balancing, thermal management, fault detection, and estimation of charge, power, and health [7]. One of the primary challenges in BMSs is achieving effective SoC balancing within a battery pack. If SoC balancing is not maintained, the battery pack can experience significant issues such as

reduced driving range, accelerated aging, and even thermal runaway [8]—a condition where a battery’s temperature increases uncontrollably, potentially leading to catastrophic failure [9].

One key solution is the implementation of passive and/or active balancing techniques for the SoC management [10, 11]. Passive balancing uses resistors to dissipate excess energy from higher-charged cells [12, 13], while active balancing employs more efficient methods to redistribute charge among cells, ensuring uniform SoC across the battery pack [14, 15].

Thermal management in BMSs combines hardware solutions (see [16] for further insights) with advanced control strategies. The BMS uses thermal sensors throughout the battery pack to monitor temperature variations in real-time [17]. Based on this data, it can activate air or liquid cooling systems to address thermal imbalances, adjusting fan speeds, airflow patterns, or coolant flow rates as needed [18, 19]. On the controller side, the BMS may adjust charging and discharging rates to minimize heat generation to fulfill thermal constraints [20]. In extreme cases, it may temporarily limit power output to prevent overheating.

Reconfigurable Battery (RB) systems, also known as modular batteries, are advanced battery energy storage systems that can dynamically adjust their internal connections and configurations [21]. These systems utilize components like DC-DC converters, H-bridge converters and Half-Bridge Converters (HBCs) to enable flexible energy management and distribution within the battery pack. The key advantages of RBs include:

- Improved SoC balancing: The ability to reconfigure connections facilitates better energy distribution and SoC balancing across the pack [22, 23].
- Efficient thermal management: Dynamic reconfiguration enables load shifting (e.g. decrease load on modules that are over-heating), contributing to better thermal management and potentially preventing thermal runaway [24].
- Fault tolerance: RBs can isolate faulty cells or modules through reconfiguration, enhancing system reliability and safety.
- Customizable voltage output: The modular nature of RBs allows for adjustable output voltage levels to suit different application requirements.

The following section provides a literature review of control strategies for reconfigurable battery systems.

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TABLE I
SUMMARY OF CONTROL STRATEGIES APPLIED TO ACTIVE BALANCING CIRCUITS.

Reference	BMS Control Approach	Balancing Hardware	Experimental Validation	Power Loss Optimization	Safety Guarantees	Implementation Complexity
[25]	Classical Feedback Controller (PI)	DC-DC Conv.	✓	✗	SoH-Aware	Low
[26]	Rule-Based	HBC	✓	✗	✗	Low/Medium
[27]	Rule-Based	HBC	✓	✓	✗	Low/Medium
[28]	Rule-Based	Not Specified	✗	✗	✗	Low
[29]	Model-Based (Optimal)	Single Conv.	✗	✓	(I, V)	High
[30]	Model-Based (MPC)	H-Bridge	✓	✓	(P)	High
[31]	Model-Based (MPC)	DC-DC Conv.	✗	✓	✗	High
[32]	Model-Based (MPC)	Multilevel Conv.	✗	✓	(SoC, T)	Medium to High
[24]	Data-Driven/Hybrid	HBC	✗	✗	(T)	Medium
[33]	Data-Driven/Hybrid	Custom RB	✗	✗	✗	Medium
[34]	Data-Driven (RL)/Hybrid	DC-DC Conv.	✗	✗	✗	Medium
Our Work	Model-Based (CA+CBF)	HBC	✓	✓	(V, T)	Medium

Conv.: Converter; SoH: State-of-Health; MPC: Model Predictive Control; RL: Reinforcement Learning; CBF: Control Barrier Function. I : current protection; V : voltage protection; P : power limits; SoC : SoC upper and lower limits; T : over-temperature protection.

A. Balancing Control Literature Review

Authors in [25] and [26] proposed Proportional Integrator (PI) and rule-based approaches to SoC balancing, respectively. These methods, implemented with DC-DC and HBC hardware, respectively, and are simple to implement but provide sub-optimal results. They are unable to handle multiple safety constraints in a systematic way, such as thermal protection; they also do not offer optimality guarantees such as power loss minimization. Data-driven approaches, such as those presented in [24] and [34], rely on input-output data of the battery and balancing hardware to develop the control algorithm. In [24], a K-Nearest Neighbor (KNN) algorithm was applied for SoC and temperature balancing using HBC, while Reinforcement Learning (RL) was employed in [34] with DC-DC converters. These approaches require large and rich datasets, and the training is computationally expensive. Another common weakness is the lack of interpretability, making it challenging to gain insight into the underlying decision processes. Model Predictive Control (MPC) has been widely used as a model-based approach [30, 31]. MPC allows for systematic handling of multiple safety constraints, such as thermal and voltage limits, and is implemented in conjunction with H-bridge and DC-DC converters for efficient balancing. By incorporating preview information and optimizing performance, MPC can achieve higher energy efficiency. In addition, aging-aware balancing controllers have been proposed to explicitly account for cell degradation during operation; notably, [35] applies nonlinear MPC, while [36] uses an optimal control strategy to extend battery life by adapting to cell heterogeneities. However, a common drawback of MPC-based approaches is their high real-time computational effort [31].

B. Contributions

Table I provides a summary of the features found in recent literature on balancing control of batteries. Ideally, we would like to have strategies that 1) offer provable safety and optimal-operation guarantees; 2) are experimen-

tally validated, and 3) are implemented with low-to-medium implementation complexity. Our analysis reveals that none of the previous literature was able to simultaneously fulfill requirements 1), 2), and 3). For example, MPC [30] can fulfill 1) and 2) but fails to meet 3). Furthermore, the control method in [32] fulfills 1) and partially 3), but lacks 2) experimental validation. In contrast, rule-based methods [26, 27] fulfill 2) and 3) but lack providing safety guarantees.

In this work, we adopt a model-based approach to control RBs combining Control Allocation (CA) [37, 38] with Control Barrier Function (CBF)-based optimal controller [39], which fulfills all the above requirements. CA is a method used to distribute the control effort, leveraging over-activation to minimize some cost function (e.g. energy losses) while fulfilling activation constraints. In the context of reconfigurable batteries, CA ensures that the reference voltage is appropriately assigned to suitable battery modules, balancing load distribution and electro-thermal safety constraints. The approach may yield multiple solutions, providing the controller with additional degrees of freedom to meet further operational constraints or optimize performance [40, 41].

CBFs have been widely applied in various domains, from automotive [42], robotics [43], to medical [44], to enforce safety constraints while optimizing control objectives, making them well-suited for addressing the safety-critical challenges in this system.

The main contribution of this paper is a novel CA+CBF formulation for the safe control of reconfigurable battery systems. The proposed formulation is posed as a lightweight quadratic optimization problem that simultaneously performs voltage allocation, SoC balancing, and over-temperature protection, while minimizing power losses. We provide a theoretical analysis of the CA+CBF method and derive bounds on the CBF gains that guarantee numerical feasibility of the optimization problem, offering important insights for controller tuning. Through numerical simulations, we show that the proposed method achieves comparable levels of constraint satisfaction and optimality to state-of-the-art MPC formulations, while reducing computation time by more than

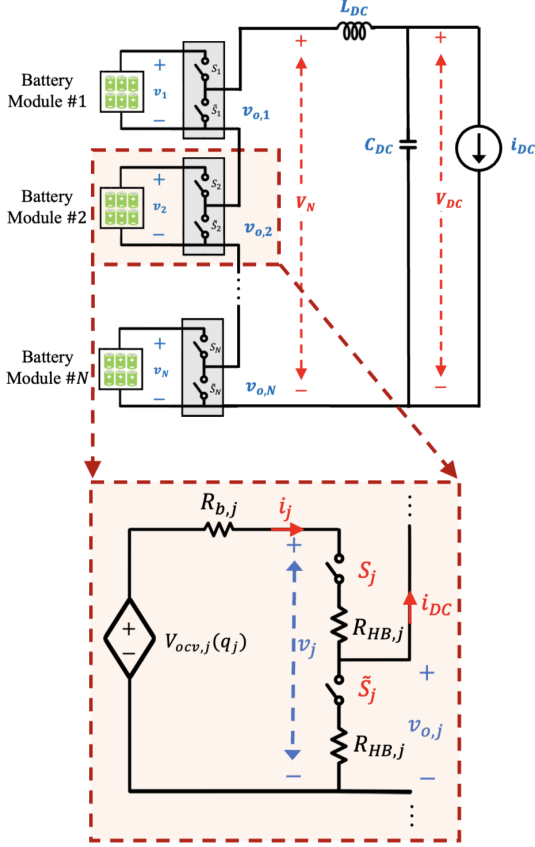


Fig. 1. Overview of the reconfigurable battery system, with simplified battery and half-bridge converters [45].

60%. Finally, we validate the proposed control strategy on an experimental prototype, demonstrating its feasibility and effectiveness in a practical (small-scale) reconfigurable battery system.

This paper expands our previous work [45], offering both theoretical analysis of the controller properties and practical implementations, supported by experimental results.

The paper is organized as follows: Section II provides a modeling overview of the battery system, used in control design and simulations. Section III outlines the control objectives, scheme, and feasibility of the CA+CBF-based controller. Section IV compares its performance to a baseline MPC controller, including tuning, scalability, and key performance indicators. Experimental validation is detailed in Section V, and conclusions are presented in Section VI.

II. MODELING

This section presents the proposed architecture of the reconfigurable battery design. We assume that there are N battery modules, composed of multiple cells connected in parallel and series to form the module $j = \{1, 2, \dots, N\}$. Each battery module is attached to a HBC as depicted in Fig. 1.

TABLE II
COMPACT MODEL PARAMETER DESCRIPTION.

Variable	Symbol	Definition
Battery Resistance	\mathbf{R}_b	$[R_{b,1}, \dots, R_{b,N}]^\top$
Battery Capacity	\mathbf{C}_{bat}	$\text{diag}([C_1, \dots, C_N])$
Battery SoC	\mathbf{Q}	$[Q_1, \dots, Q_N]^\top$
Battery OCV	\mathbf{V}_{ocv}	$[v_{\text{ocv},1}, \dots, v_{\text{ocv},N}]^\top$
Battery Current	\mathbf{I}	$[I_1, \dots, I_N]^\top = i_{DC} \mathbf{u}$
Battery Voltage	\mathbf{V}	$\mathbf{V}_{\text{ocv}} - \text{diag}(\mathbf{R}_b) i_{DC} \mathbf{u}$
Battery Temp.	\mathbf{T}	$[T_1, \dots, T_N]^\top$
Thermal Capacity	\mathbf{C}_T	$\text{diag}[C_{T,1}, \dots, C_{T,N}]$
CTR*	\mathbf{R}_C	$\text{diag}([R_{C,1}, \dots, R_{C,N}])$
Ambient Temp.	\mathbf{T}_a	$T_a \mathbf{1}_N^{**}$
HBC Model		
HBC Resistance	\mathbf{R}_{HB}	$[R_{\text{HB},1}, \dots, R_{\text{HB},N}]^\top$
HBC Output V.	\mathbf{V}_o	$\text{diag}(\mathbf{u}) \mathbf{V} - \mathbf{R}_{\text{HB}} i_{DC}$

* CTR: Convective Thermal Resistance

** $\mathbf{1}_N$ is a unity vector of dimension $N \times 1$.

When the upper switch of the HBC is active ($S_j = 1$), the battery is connected to the output, and when the lower switch is active $\tilde{S}_j = 1$, the battery is bypassed. Both switches cannot be closed at the same time, which results in battery short-circuit. The HBCs are further connected to an LC filter to smooth the output voltage and a current source is used to emulate the electrical load (e.g., a motor inverter in an electric vehicle application).

A. Compact Average Model Representation

As depicted in Fig. 1, each battery module is modeled as an open circuit voltage (OCV) voltage source dependent on the SoC, in series with an internal resistance $R_{b,j}$. The HBC's switches operate with a pulse-width modulator, where $m_j \in [0, 1]$ denotes the fraction of time that the battery module j is connected to the load. To simplify modeling, we further consider average values for the battery current (\mathbf{I}) and output voltage of the HBC ($v_{o,j}$) over a switching period [46, Section 4.4].

The battery and HBC model is compactly represented as:

$$\frac{d}{dt} \mathbf{Q} = -\mathbf{C}_{\text{bat}}^{-1} i_{DC} \mathbf{u}, \quad (1a)$$

$$\begin{aligned} V_N &= \mathbf{1}_N^\top \mathbf{V}_o = \mathbf{u}^\top \mathbf{V}_{\text{ocv}} - \\ &\quad - \mathbf{u}^\top \text{diag}(\mathbf{R}_b) i_{DC} \mathbf{u} - \mathbf{1}_N^\top \mathbf{R}_{\text{HB}} i_{DC}, \end{aligned} \quad (1b)$$

$$\mathbf{C}_T \frac{d}{dt} \mathbf{T} = -\mathbf{R}_C^{-1} (\mathbf{T} - \mathbf{T}_a) + \mathbf{u}^\top \text{diag}(\mathbf{R}_b) i_{DC}^2 \mathbf{u}, \quad (1c)$$

$$P_l(\mathbf{u}) = \mathbf{u}^\top \text{diag}(\mathbf{R}_b) i_{DC}^2 \mathbf{u} + \mathbf{1}_N^\top \mathbf{R}_{\text{HB}} i_{DC}^2, \quad (1d)$$

where $\mathbf{u} = [m_1, m_2, \dots, m_N]^\top$ represent the vector of duty cycles applied to the HBCs. All the remaining parameters/states of this model are defined in Table II. The first equation models the SoC (\mathbf{Q}) of each battery module. The second equation captures the average output that is generated by the HBC and denoted V_N . The third equation captures the

temperature response of the battery modules using a lumped thermal model. The last equation models the power losses (P_l) within the internal resistance of the batteries and the HBC.

Remark 1: In this work, the battery module is modeled using an open-circuit voltage as a function of SoC in series with an internal resistance, neglecting dynamic effects. The advantage of this simplified model is the ease of use: we only need the steady-state characterization of the battery module, which can be obtained via datasheets or experiments [47, 48]. While more accurate models could be used, e.g. equivalent circuit models with one (or more) RC pairs or electro-chemical representations, this increases the implementation and modeling complexity and effort, requiring additional calibration effort. Our idea is to deploy a low-dimension easy-to-parameterize battery model and then rely on the inherent robustness capabilities of the CBFs to deal with model uncertainties [49]. Extending the framework to include battery dynamics is conceptually straightforward and is left for future work.

III. CONTROL DESIGN

Our objective is to find the duty cycles $\mathbf{u} = [m_1, \dots, m_N]^T$ in order to fulfill the following requirements:

- (i) Input constraints, i.e. $\mathbf{u} \in U = [0, 1]^N$;
- (ii) Control of output voltage, i.e. $V_{DC} \rightarrow V_{DC}^*$, where V_{DC}^* is the desired voltage;
- (iii) SoC balancing, i.e. $|Q_j - Q_k| \leq \Delta Q_{max}$ for any $j \neq k$ where ΔQ_{max} is the tolerance for charge imbalance;
- (iv) Temperature limits: $\mathbf{T} \leq T_{max} \mathbf{1}_N$;
- (v) Minimize power losses $P_l(\mathbf{u})$.

Fig. 2 represents the control diagram that we used to address the control requirements. This design is divided into two layers. The first layer focuses on control of the output voltage (V_{DC}) by manipulation of a reference value for the HBC's output voltage (V_{ref}). The second layer is responsible for generating the duty cycle \mathbf{u} capable of fulfilling generating V_{ref} while enforcing safety constraints.

A. Outer Control: Voltage Control

Let us consider V_{ref} as the desired value for V_N (aka as “virtual control” input in the CA [38]). In this work, we employ a PI to make V_{DC} follow V_{DC}^* via manipulation of V_{ref} :

$$V_{ref} = K_p(V_{DC} - V_{DC}^*) + K_i Z, \quad (2a)$$

$$\dot{Z} = V_{DC} - V_{DC}^*, \quad (2b)$$

where K_p and K_i are the proportional and integrator control gains, respectively, which can be tuned, for example via pole placement [50].

B. Inner Control Design

This section presents the design of the inner control layer, which relies on CA for allocation of the voltage (V_{ref}) and CBF for enforcement of SoC and temperature constraints.

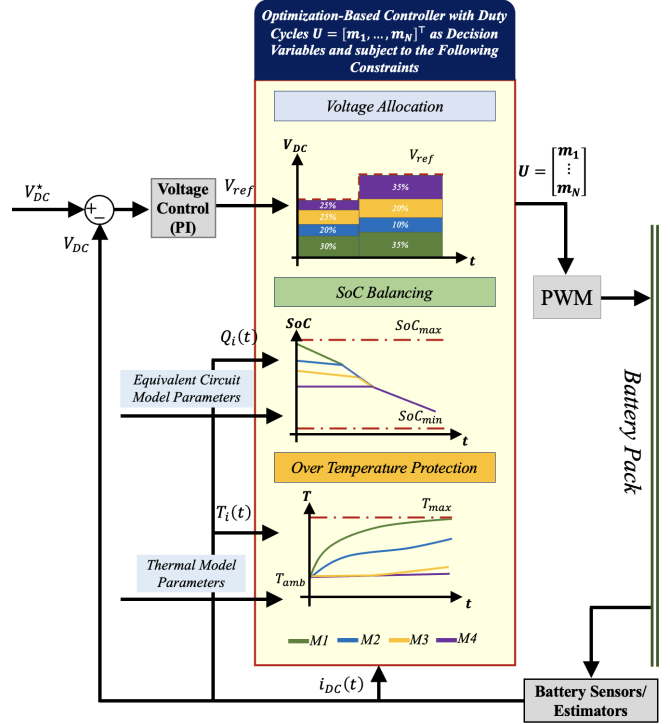


Fig. 2. Overview of the control architecture, composed of an outer voltage control, inner controller, PWM, and sensor/estimators.

1) *Voltage Allocation:* To fulfill the reference voltage requested by the high-level controller, we will need to find a \mathbf{u} that lies in the following set:

$$\mathcal{U}_V = \{ \mathbf{u} \in U : V_{ref} = \mathbf{u}^T (\mathbf{V}_{ocv} - \text{diag}(\mathbf{R}_b) i_{DC} \mathbf{u}) - \mathbf{1}_N^T \mathbf{R}_{HB} i_{DC} \} \quad (3)$$

Note that \mathcal{U}_V is defined by a quadratic constraint on \mathbf{u} that may be under-determined, i.e., a constraint that has more unknowns than constraints. As a result \mathcal{U}_V may have more than one element, which is a typical feature in control allocation problems. We will leverage these multitude of solutions to enforce SoC and temperature constraints.

2) *SoC Balancing Constraints:* The SoC balancing will make use of CBF techniques.

Let us consider two neighbor modules k and $k+1$. Our goal is to have a battery pack that is equalized (at module level) with a tolerance ΔQ_{max} . Mathematically, this means forcing the SoC (\mathbf{Q}) to stay inside the following set¹:

$$\mathcal{Q} = \{ \mathbf{Q} : |Q_k - Q_{k+1}|^2 \leq \Delta Q_{max}^2, \quad k = 1 \dots N \}. \quad (4)$$

To facilitate the CBF application, it is convenient to rewrite these constraints as positive (safety) inequalities for each $k = 1, \dots, N$:

$$\tilde{c}_k(\mathbf{Q}, \Delta Q_{max}) = -(Q_k - Q_{k+1})^2 + \Delta Q_{max}^2 \geq 0. \quad (5)$$

To enforce these positive inequalities, we make use of zeroing control barrier functions [51]. The idea is to compute a set of

¹We adopt the following notation abuse: $Q_{N+1} = Q_1$.

safe control actions that promote the fulfillment of the safety constraints $\tilde{c}_k(\mathbf{Q}) \geq 0$. This can be computed as:

$$\mathcal{U}_Q(\mathbf{Q}) = \{\mathbf{u} \in U : \dot{\tilde{c}}_k(\mathbf{Q}, \mathbf{u}) \geq -\alpha_k(\tilde{c}_k(\mathbf{Q})), k = 1, \dots, N\}, \quad (6)$$

where $\alpha_k(\cdot)$ is an extended class \mathcal{K} [52] function that can be tuned by the user. Note that:

$$\dot{\tilde{c}}_k(\mathbf{Q}) = \frac{\partial \tilde{c}_k}{\partial \mathbf{Q}} \frac{\partial \mathbf{Q}}{\partial t} = -\frac{\partial \tilde{c}_k}{\partial \mathbf{Q}} \mathbf{C}_{\text{bat}}^{-1} i_{DC} \mathbf{u}. \quad (7)$$

Hence, the safe input set can be expressed as a set of linear inequalities on \mathbf{u} :

$$\mathcal{U}_Q(\mathbf{Q}) = \{\mathbf{u} \in U : \mathbf{B}_k \mathbf{u} \geq -\alpha_k(\tilde{c}_k(\mathbf{Q})), k = 1, \dots, N\}, \quad (8)$$

where $\mathbf{B}_k = -\frac{\partial \tilde{c}_k}{\partial \mathbf{Q}} \mathbf{C}_{\text{bat}}^{-1} i_{DC}$.

3) *Temperature Constraints*: let us consider the upper-temperature limit constraint for each module:

$$\mathcal{T} = \{\mathbf{T} \in \mathbb{R}^N : T_k \leq T_{max}, k = 1, \dots, N\}. \quad (9)$$

These limits can be translated into the following positive inequalities:

$$c_k(T_k, T_{max}) = -T_k + T_{max} \geq 0, \quad (10)$$

for $k = 1, \dots, N$. To enforce these constraints, we again make use of zeroing CBFs. The set of safe control inputs that guarantee fulfillment of temperature constraint is defined as:

$$\mathcal{U}_T(\mathbf{T}) = \{\mathbf{u} \in U : \dot{c}_k(\mathbf{T}, \mathbf{u}) \geq -\beta_k(c_k(\mathbf{T})), k = 1, \dots, N\}, \quad (11)$$

where $\beta_k(\cdot)$ is an extended class \mathcal{K} function defined by the user. By expanding the derivative \dot{c}_k , this safety input set can be re-written as a set of quadratic inequalities on u_k :

$$\mathcal{U}_T(\mathbf{T}) = \{\mathbf{u} \in U : \frac{T_k - T_a}{C_{T,1} R_{C,1}} - \frac{R_{T,k}}{C_{T,k}} i_{DC}^2 u_k^2 \geq -\beta_k(c_k(\mathbf{T})), k = 1, \dots, N\}. \quad (12)$$

Based on the above safety framework, our allocation and safety problem can be re-stated as finding a safe and feasible $\mathbf{u} = U \cap \mathcal{U}_V \cap \mathcal{U}_Q \cap \mathcal{U}_T$ that minimize the power losses $P_l(\mathbf{u})$. This can be translated into the following optimization problem:

$$\underset{\mathbf{u}}{\text{minimize}} \quad \mathcal{J}_{\text{CA+CBF}}(\mathbf{u}) \quad (13a)$$

subject to

$$\mathbf{u} \in U = [0, 1]^N, \quad (13b)$$

$$\mathbf{u}^\top \mathbf{V}_{\text{ocv}} - \mathbf{u}^\top \text{diag}(\mathbf{R}_b) i_{DC} \mathbf{u} - \mathbf{1}_N^\top \mathbf{R}_{\text{HB}} i_{DC} = V_{ref} + \delta_V, \quad (13c)$$

$$\mathbf{B}_k \mathbf{u} \geq -\alpha_k(\tilde{c}_k(\mathbf{Q}, \Delta Q_{max} + \delta_{Q,k})), \quad (13d)$$

$$\frac{T_k - T_a}{C_{T,k} R_{C,k}} - \frac{R_{T,k}}{C_{T,k}} i_{DC}^2 u_k^2 \geq -\beta_k(c_k(\mathbf{T}, T_{max} + \delta_{T,k})), \quad (13e)$$

$$0 \leq \delta_V, \quad 0 \leq \delta_{Q,k}, \quad 0 \leq \delta_{T,k}, \quad (13f)$$

$$k = 1, 2, \dots, N$$

Constraint (13b) enforces the input limits; (13c) enforces the output voltage allocation, where δ_V is the voltage allocation slack variable that can be used to recover the numerical feasibility of the optimization problem. Equation (13d) implements SoC balancing constraints, where $\delta_{Q,k}$ is a slack variable that enables relaxation of the specified balancing tolerance, and (13e) enforces maximum temperature constraints with the slack variable $\delta_{T,k}$ that relaxes the maximum allowed temperature.

The cost function $\mathcal{J}_{\text{CA+CBF}}(\cdot)$ aims to simultaneously minimize the power losses and the value of the slack variables:

$$\omega_1 P_l(\mathbf{u}) + \omega_2 \delta_V^2 + \omega_3 \sum \delta_{Q,k}^2 + \omega_4 \sum \delta_{T,k}^2. \quad (14)$$

Parameters ω_1 , ω_2 , ω_3 , and ω_4 are weights defined by the designer that aim to penalize power losses, and non-zero values of the slack variables.

C. Analysis: Theoretical Feasibility of Temperature CBF

From a practical perspective, it is important to understand under what conditions problem (13) is intrinsically feasible. In other words, we are interested in finding conditions under which $U \cap \mathcal{U}_V \cap \mathcal{U}_Q \cap \mathcal{U}_T \neq \emptyset$.

Assuming a linear extended class \mathcal{K} function $\beta_k(c_k) = K_T c_k$, with $K_T > 0$, then (13e) reads as

$$-\theta_2 i_{DC}^2 u_k^2 \geq -K_T(-T_k + T_{max}) - \theta_1(T_k - T_a), \quad (15)$$

where $\theta_1 = \frac{1}{R_C C_T}$ and $\theta_2 = \frac{R_b}{C_T}$ are the thermal-related parameters. To further simplify the analysis, let us introduce the following change of variable,

$$T_k = T_a + \Delta T_k, \quad T_{max} = T_a + \overline{\Delta T}_k, \quad (16)$$

where ΔT_k correspond to the temperature increase of module k above ambient temperature and $\overline{\Delta T}_k$ the maximum allowed increase for this battery module. The set of thermally safe control inputs can be re-written as:

$$\mathcal{U}_T(\Delta T_k) = \left\{ \mathbf{u} \in U : u_k^2 \leq \frac{\theta_1 - K_T}{\theta_2 i_{DC}^2} \Delta T_k + \frac{K_T}{\theta_2 i_{DC}^2} \overline{\Delta T}_k \right\}. \quad (17)$$

Theorem 1. Assume that $T_k \geq T_a$ (or $\Delta T_k \geq 0$) and $i_{DC} \neq 0$. The safe input set $\mathcal{U}_T(\Delta T_k)$ is feasible if

- (i) $0 \leq K_T \leq \theta_1$, for $0 \leq \Delta T_k$;
 - (ii) $\theta_1 < K_T \leq \theta_1 \frac{\Delta T^*}{\Delta T^* - \overline{\Delta T}_k}$, for $0 \leq \Delta T_k \leq \Delta T^*$,
- where $\Delta T^* > \overline{\Delta T}_k$ is a user-defined value.

Proof. The assumption $i_{DC} \neq 0$ is useful to avoid division by zero.

Case 1: Assume $K_T \leq \theta_1$, hence

$$u_k^2 = m_k^2 \leq \underbrace{\frac{\theta_1 - K_T}{\theta_2 i_{DC}^2}}_{a(K_T)} \Delta T_k + \underbrace{\frac{K_T}{\theta_2 i_{DC}^2} \overline{\Delta T}_k}_{b(K_T)} \quad (18a)$$

$$\leq a(K_T) \Delta T_k + b(K_T) = m_k^{max}(\Delta T_k). \quad (18b)$$

To guarantee feasibility of \mathcal{U}_T we need to find \mathbf{u} that fulfills $0 \leq u_k \leq \min(1, \sqrt{m_k^{max}(\Delta T_k)})$ for all $\Delta T_k \geq 0$. Note that

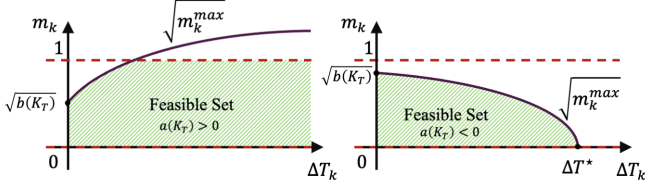


Fig. 3. Pictorial representation of the (temperature) safe control set $\mathcal{U}_T(\Delta T_k)$, for the two cases of $K_T \leq \theta_1$ on the left, and $K_T > \theta_1$ on the right.

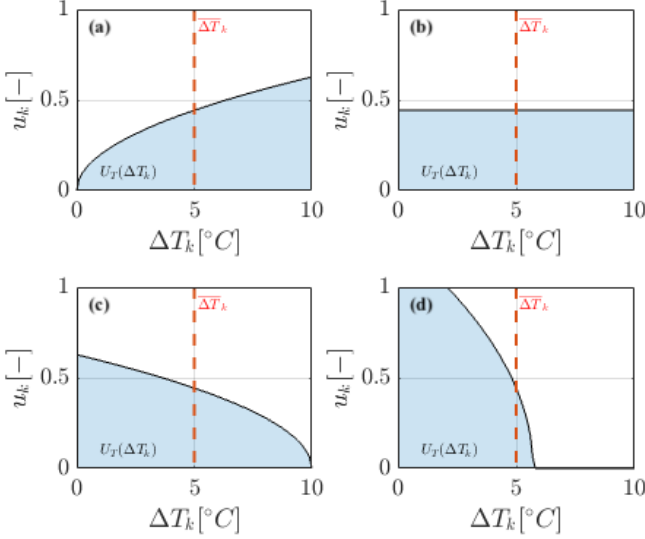


Fig. 4. Illustration of the (temperature) safe control set $\mathcal{U}_T(\Delta T_k)$ for different values of the tuning parameter K_T . Note: the plot was generated assuming $i_{DC} = 2A$ and $\overline{\Delta T}_k = 5^\circ C$. (a) $K_T = 0.0\theta_1$, (b) $K_T = 1.0\theta_1$, (c) $K_T = 2.0\theta_1$, and (d) $K_T = 8.0\theta_1$.

both $a(K_T)$ and $b(K_T)$ are positive functions. As a result, the upper bound $m_k^{max}(\Delta T_k)$ is a positive increasing function for ΔT_k and we can always find a feasible \mathbf{u} (see Fig. 3-left).

Case 2: In this case, $K_T > \theta_1$, hence $a(K_T)$ is negative, and $b(K_T) \geq 0$. This means that the upper bound $m_k^{max}(\Delta T_k)$ is a decreasing function (see Fig. 3-right). Our goal is to ensure that $m_k^{max}(\Delta T_k)$ remains positive in the domain $0 \leq \Delta T_k \leq \Delta T^*$, thus promoting feasibility of \mathcal{U}_T . Since $m_k^{max}(\Delta T_k)$ is a decreasing function, we just need to check the feasibility condition when $\Delta T_k = \Delta T^*$:

$$0 \leq a(K_T)\Delta T^* + b(K_T). \quad (19)$$

Expanding $a(K_T)$ and $b(K_T)$:

$$0 \leq \frac{\theta_1 - K_T}{\theta_2 i_{DC}^2} \Delta T^* + \frac{K_T}{\theta_2 i_{DC}^2} \overline{\Delta T}_k. \quad (20)$$

This inequality can be re-arranged as:

$$K_T \leq \theta_1 \frac{\Delta T^*}{\Delta T^* - \overline{\Delta T}_k}, \quad (21)$$

which concludes the proof. \square

Remark 2: Fig. 4 shows $\mathcal{U}_T(\Delta T_k)$ for different values of K_T and ΔT_k . The results illustrate that picking large ‘‘CBF

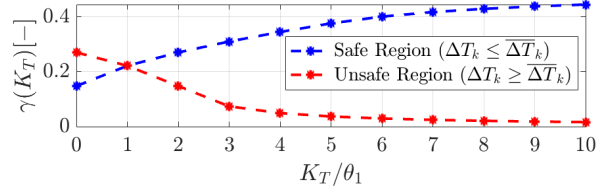


Fig. 5. Comparison of the normalized surface area of the (thermal) safe and unsafe control set (separated by the threshold and $\overline{\Delta T}_k$) for different gains $K_T = G\theta_1$. (blue curve $\gamma^{safe}(K_T)$, red curve $\gamma^{unsafe}(K_T)$)

gains’’ ($K_T > \theta_1$) enlarges the safe control set $\mathcal{U}_T(\Delta T_k)$ when the state is inside the safe set ($\Delta T_k \leq \overline{\Delta T}_k$); but the control set quickly ‘‘shrinks’’ when the constraint is violated ($\Delta T_k > \overline{\Delta T}_k$), leading to numerical infeasibility issues. To attenuate this, the user can pick ‘‘low CBF gains’’ ($K_T < \theta_1$), which usually attenuate the numerical infeasibility problems outside the safe set ($\Delta T_k > \overline{\Delta T}_k$), but make the CBF more restrictive inside the safe set, affecting system performance even when the state is far away from the boundary of the safety set. To quantify this tuning trade-off, Fig. 5 represents the normalized size of the safe control sets:

$$\gamma^{safe}(K_T) = \frac{\int_0^{\overline{\Delta T}_k} \max(0, m_k^{max}(\Delta T_k)) d\Delta T_k}{\int_0^{\overline{\Delta T}_k} 1 d\Delta T_k}, \quad (22)$$

and the normalized size of the unsafe control set:

$$\gamma^{unsafe}(K_T) = \frac{\int_{\overline{\Delta T}_k}^{\overline{\Delta T}_k^{max}} \max(0, m_k^{max}(\Delta T_k)) d\Delta T_k}{\int_{\overline{\Delta T}_k}^{\overline{\Delta T}_k^{max}} 1 d\Delta T_k}, \quad (23)$$

where $m_k^{max}(\Delta T_k)$ is the maximum (safe) allowed duty cycle allowed by the CBF defined in the Proof of Theorem 1 and $\overline{\Delta T}_k^{max}$ is the maximum temperature range. The metric $\gamma^{safe}(K_T)$ represents the (normalized) size of the safe input set when the temperature constraint is fulfilled, while $\gamma^{unsafe}(K_T)$ captures the (normalized) when the temperature constraint is violated. Fig. 5 shows the trade-off between these two metrics: as K_T increases, $\gamma^{safe}(K_T)$ becomes larger and less conservative (inside the safe set), but $\gamma^{unsafe}(K_T)$ shrinks, which may create numerical feasibility issues when the temperature constraint is violated.

Remark 3: Additionally, we also found out the existence of an invariant point. To understand this, note that $\mathcal{U}_T(\Delta T_k)$ depends on the function $m_k^{max}(\Delta T_k)$, which defines the maximum duty cycle for a certain temperature increase and is defined as (see Proof of Theorem 1):

$$m_k^{max}(\Delta T_k) = \frac{\theta_1 - K_T}{\theta_2 i_{DC}^2} \Delta T_k + \frac{K_T}{\theta_2 i_{DC}^2} \overline{\Delta T}_k. \quad (24)$$

At the limit of the (temperature) safe set, we obtain:

$$m_k^{max}(\overline{\Delta T}_k) = \frac{\theta_1}{\theta_2 i_{DC}^2} \overline{\Delta T}_k. \quad (25)$$

Note that this point does not depend on the selection of the CBF gain and it is invariant with respect to K_T . This

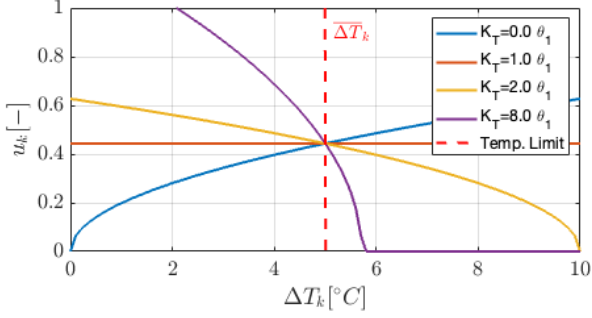


Fig. 6. Representation of the maximum allowed control input $m_k^{max}(\Delta T_k, K_T)$ that is used to construct \mathcal{U}_T . Note: the plot was generated assuming $i_{DC} = 2A$ and $\Delta \bar{T}_k = 5^\circ C$.

means that the feasibility of the CBF when $\Delta T_k = \Delta \bar{T}_k$ does not depend on the tuning of the CBF. Instead, it is dictated by the value of the DC current i_{DC} . Large values of i_{DC} decrease $m_k^{max}(\Delta \bar{T}_k)$ and make the (temperature) CBF more restrictive. This is in line with our expectations: the CBF will tend to decrease the duty cycle when large DC currents (which lead to greater heat generation) are requested.

D. Analysis: Theoretical Feasibility of SoC Balancing CBF

Now, let us look into the feasibility of \mathcal{U}_Q . We divide the analysis into the two cases: 1) $\mathbf{Q} \in \mathcal{Q}$, hence $\tilde{c}_k(\mathbf{Q}) \geq 0$, and 2) $\mathbf{Q} \notin \mathcal{Q}$, i.e. $\tilde{c}_k(\mathbf{Q}) < 0$.

1) Case 1:

Lemma 1. $\mathcal{U}_Q(\mathbf{Q}) \neq \emptyset$ for all $\mathbf{Q} \in \mathcal{Q}$.

Proof. We will consider $\mathbf{u} = 0$ as a candidate control action to enforce \mathcal{Q} . The control $\mathbf{u} = 0$ is feasible as long as

$$\mathbf{B}_k \mathbf{0} \geq -\alpha_k(\tilde{c}_k(\mathbf{Q})). \quad (26)$$

Since we assume that $\mathbf{Q} \in \mathcal{Q}$, then $\tilde{c}_k(\mathbf{Q}) \geq 0$. Additionally, α_k is an extended class \mathcal{K} function [52], thus $\alpha_k(\zeta) \geq 0$ when $\zeta \geq 0$. Hence, the right side of (26) is non-positive

$$0 \geq -\alpha_k(\tilde{c}_k(\mathbf{Q})), \quad (27)$$

for all $\mathbf{Q} \in \mathcal{Q}$, which allow us to verify condition (26). \square

2) Case 2: the feasibility conditions for \mathcal{U}_Q are slightly more involved when $\mathbf{Q} \notin \mathcal{Q}$, which implies that $\tilde{c}_k(\mathbf{Q}) < 0$. To understand this, let us re-write this condition as:

$$\tilde{c}_k(\mathbf{Q}) = -\Delta Q_k^2 + \Delta Q_{max}^2 < 0, \quad (28)$$

where $\Delta Q_k = Q_{k+1} - Q_k$ is the SoC imbalance between two cells. Let us assume a linear extended class \mathcal{K} function: $\alpha_k(\zeta) = K_{Q,k} \zeta$ where $K_{Q,k} > 0$ is a user-defined gain. Hence, the CBF constraint (8) will read as

$$\mathbf{B}_k \mathbf{u} \geq -K_{Q,k} \tilde{c}_k(\mathbf{Q}) \quad (29a)$$

$$\geq K_{Q,k} (\Delta Q_k^2 - \Delta Q_{max}^2). \quad (29b)$$

Let us expand the left side of the inequality into a scalar representation:

$$\mathbf{u} \in U, \quad \sum_j B_{kj} u_j \geq K_{Q,k} (\Delta Q_k^2 - \Delta Q_{max}^2), \quad (30)$$

where $B_{kj} = -\frac{\partial \tilde{c}_k}{\partial Q_j} C_{bat,j}^{-1} i_{DC}$. Recall that $U \in [0, 1]^N$. In order to seek a feasible control input (i.e. maximize the left side of the previous inequality), it is convenient to pick $u_j = 1$ if B_{kj} is positive, and zero ($u_j = 0$) otherwise. Therefore

$$\sum_j B_{kj} \mathbf{1}_{\{B_{kj} \geq 0\}} \geq K_{Q,k} (\Delta Q_k^2 - \Delta Q_{max}^2). \quad (31)$$

Assuming a maximum tolerable SoC imbalance, referred to as $\bar{\delta}_Q$, and $\Delta Q_{max}^2 < \Delta Q_k^2 \ll \bar{\delta}_Q^2$, then

$$0 < K_{Q,k} \leq \frac{\sum_j B_{kj} \mathbf{1}_{\{B_{kj} \geq 0\}}}{\bar{\delta}_Q^2}. \quad (32)$$

With further expansion

$$0 < K_{Q,k} \leq \frac{\sum_j \tilde{B}_{kj} \mathbf{1}_{\{\tilde{B}_{kj} \geq 0\}}}{\bar{\delta}_Q^2} |i_{DC}| = \theta_{3,k}, \quad (33)$$

where $\tilde{B}_{kj} = -\frac{\partial \tilde{c}_k}{\partial Q_j} C_{bat,j}^{-1} \text{sign}(i_{DC})$.

The following Theorem summarizes the conditions that preserves feasibility of $\mathcal{U}_Q(\mathbf{Q})$:

Theorem 2. If $\tilde{c}_k(\mathbf{Q}) \geq 0$, then the CBF constraint (8) is feasible, for any gain $K_{Q,k}$. Else if $\tilde{c}_k(\mathbf{Q}) < 0$, then the input set $\mathcal{U}_Q(\mathbf{Q})$ is feasible if (33) holds, considering a maximum SoC imbalance $\bar{\delta}_Q$, and $i_{DC} \neq 0$.

Proof. Lemma 1 and Case 2 analysis provide the proof of this Theorem. \square

Remark 4: The results presented in Theorem 1 provide bounds for the maximum CBF gains (K_T) that the user can employ in practice without compromising numerical feasibility of the CBF optimization problem within the expected operation range of the battery temperature ($\Delta T_k \leq \Delta T^*$). The same applies to Theorem 2 and $K_{Q,k}$. We believe these bounds have both theoretical and practical value for the application of the CBF to reconfigurable batteries, where the control engineer needs clear tuning guidelines for the CBF gains. If the bounds of the Theorems are violated, there will be some points in the operating range of the battery where the safe input set is empty ($\mathcal{U}_T = \emptyset$), causing numerical issues for the optimizer (if the battery reaches those operating points). In this case, the optimizer will need to rely on “slack” variables ($\delta_{Q,k}, \delta_{T,k}$) to recover the numerical feasibility.

E. Reachable Output Voltages

In addition to the safe input sets, it is also important to understand the set of reachable reference voltages that the system can generate. Mathematically, this means computing the set

$$\begin{aligned} \mathcal{V}_{ref}(\mathbf{Q}, i_{DC}) = \{V_{ref} \in \mathbb{R} : \\ V_{ref} = \mathbf{u}^T (\mathbf{V}_{ocv}(\mathbf{Q}) - \text{diag}(\mathbf{R}_b) i_{DC} \mathbf{u}) - \\ - \mathbf{u}^T (\text{diag}(\mathbf{R}_{HB}) \mathbf{1}_N i_{DC}), u \in U\}. \end{aligned} \quad (34)$$

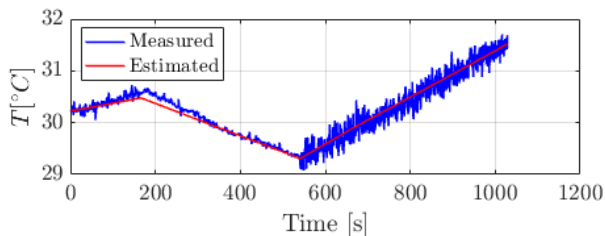


Fig. 7. Validation of the battery thermal model parameter identification.

Deriving closed-form expressions for this set is not straightforward. In this work, we adopt a pragmatic approach that approximates the reachable set as:

$$\mathcal{V}_{ref} \approx [V_{ref}^{min}, V_{ref}^{max}], \quad (35)$$

where V_{ref}^{min} , V_{ref}^{max} correspond to the minimum and maximum limits for the output voltage. We estimate V_{ref}^{min} under the worst-case maximum load current i_{dc}^{max} (which leads to higher voltage drops due to parasitic resistances) and full utilization of all battery modules ($\mathbf{u} = \mathbf{1}_N$):

$$V_{ref}^{min}(\mathbf{Q}) = \mathbf{1}_N^T (\mathbf{V}_{ocv}(\mathbf{Q}) - \text{diag}(\mathbf{R}_b) i_{dc}^{max} \mathbf{1}_N) - \mathbf{1}_N^T (\text{diag}(\mathbf{R}_{HB}) \mathbf{1}_N i_{dc}^{max}).$$

A similar maximum bound V_{ref}^{max} is computed assuming minimum current.

IV. NUMERICAL RESULTS

This section illustrates the effectiveness of the proposed control architecture via numerical simulations. We initially consider three battery modules, $N = 3$, each consisting of one battery cell, representing the module. We assume all battery cells have the same chemistry and are all at the beginning of life. All the parameters of the equivalent circuit battery model and their initial states and the HBC internal resistance are summarized in Table III.

The electrical model parameters of the battery (R_b , C_{bat} , V_{nom} , V_{OCV}) are taken from the datasheet of the SAMSUNG INR21700-50E (with nominal capacity 4900 mAh) [47, 48]. The thermal model parameters (C_T , R_C) are identified using a least-squares method based on experimental thermal data of the cell (see Fig. 7). To evaluate the effectiveness of the proposed SoC balancing strategy, the cells are initialized with different initial SoC values and distinct initial temperatures. The initial variations in the SoC and initial temperature emulates the cell-to-cell variation that could appear during discharge without active balancing. The resistance of the half-bridge converter is from its datasheet [53]. And lastly, the inductance L and capacitance C values were selected based on the desired cutoff frequency $f_c = 1/(2\pi\sqrt{LC}) \approx 1\text{kHz}$, ensuring sufficient attenuation of high-frequency switching harmonics of the HBC.

All the simulations were conducted in the MATLAB/Simulink/Simscape environment Version R2024a (on a personal computer with the specifications: Apple MacBook Pro

TABLE III
BATTERY SYSTEM MODEL PARAMETERS.

Parameter	Symbol	Value	Unit
Cell Resistance	R_b	30	[mΩ]
Cell Capacity	C_{bat}	4.9	[Ah]
Cell Nominal Voltage	V_{nom}	3.6	[V]
Initial SoC	Q_{init}	$\in [75, 100]$	[%]
Ambient Temp.	T_a	23	[°C]
Initial Temp.	T_{init}	$\in [T_{amb}, T_{amb} + 3]$	[°C]
Thermal Capacity	C_T	4.68	[J/K]
CTR*	R_C	211.94	[K/W]
HBC Resistance	R_{HB}	5	[mΩ]
Filter Inductance	L_{DC}	130	[μH]
Filter Capacitance	C_{DC}	220	[μF]
Desired Setpoints			
Ref. Load Voltage	V_{DC}^*	10	[V]
Max. SoC Variation	ΔQ_{max}	0.1	[%]
Max. Allowed Temp.	T_{max}	33	[°C]
V-Control Gains			
PI Gains	$[K_p, K_i]$	[0.7, 1.5]	-
CBF Gains and Cost Function Weights			
Temperature CBF	$K_{T,k} \forall k$	0.01	-
SoC CBF	$K_{Q,k} \forall k$	10	-
Power Loss Gain	ω_1	0	-
Voltage Slack	ω_2	10^5	-
SoC Slack	ω_3	10^3	-
Temperature Slack	ω_4	10^{15}	-

* CTR: Convective Thermal Resistance

with M2Pro Chip and 16GB memory), and the optimization formulations were implemented through the YALMIP framework [54]. The sampling time for the simulations was $T_s = 0.1\text{s}$, and the optimization problems were solved using the “gurobi” solver [55].

In the following, we illustrate three test cases: 1) No inner control, where the duty cycle is computed as $m_k = \frac{V_{ref}}{NV_{max}}$, 2) MPC, which is our baseline controller (see Appendix A for details), and 3) CA+CBF.

For the tests presented in this paper, we enforced a constant voltage of $V_{DC}^* = 10\text{V}$ through the outer loop controller and emulated a driving cycle current profile. The FTP75 driving cycle was simulated using the framework described in [56], and the requested power from the battery pack was computed during the simulation see Fig. 8. The corresponding profile was then scaled down with a factor of 1 : 2123 to match our (mini) battery pack size.

A. Comparison of Controllers

1) *No inner controller*: The top row of Fig. 9 represents the battery discharge under no inner control strategy. The battery is discharged in 33.3 minutes. Since this controller does not offer any safety guarantee, we can observe that

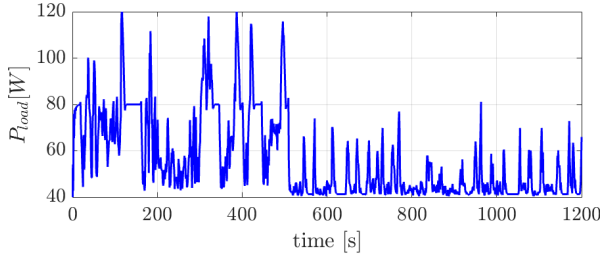


Fig. 8. Scaled FTP75 power profile obtained from the data provided in [56].

the temperature of the battery modules exceed its maximum limit. No SoC balancing is provided either.

2) *MPC Baseline Controller*: Next, we implemented a constrained optimization problem using MPC to meet load requirements, enforce cell SoC balancing, and maintain the maximum temperature limit. The details of this controller are outlined in Appendix A. Middle row of Fig. 9 illustrates the effectiveness of this control strategy, showcasing a control horizon of $H = 3$ step (with MPC sampling time of 1 second).

3) *CA+CBF Controller*: The results from the CA+CBF control strategy are presented in the bottom row of Fig. 9.

Both MPC and CA+CBF show similar results in utilizing the HBC switches to deliver the load power while reducing SoC imbalances and maintaining a safe temperature limit on each battery cell. In the initial 150 seconds, the SoC of the batteries are equalized until the first temperature constraint becomes active by reaching the proximity of T_{max} . Due to the cost function weights of the optimization problems in both MPC and CA+CBF-based controllers, temperature slack variable minimization has been given higher importance than SoC balancing ($\omega_4 \gg \omega_i, i = 1, 2, 3$). Once the first module reaches its maximum temperature limit, its duty cycle is reduced to preserve the thermal safety (see the $M1$ control signal in both control scenarios, second (b) and third row (c), first column of Fig. 9). This causes SoC imbalances in the battery pack, in order to limit the maximum temperature limit of the battery pack. We believe that this loss of SoC balancing is an acceptable compromise in order to preserve overheating conditions (which may compromise battery safety and lead to thermal runaway events).

This approach underscores the CA+CBF controller's efficacy in dynamically adjusting the HBC duty cycles to varying thermal and load conditions to ensure safety.

B. Assessment of the CBF Feasibility Guarantees

In this section, we evaluate the theoretical guarantees of the CBF-based controller. Theorems 1 and 2 provide practical bounds on the CBF gains that ensure the feasibility of the constraints and forward invariance of the safety sets.

1) *Temperature CBF*: based on the model parameters in Table III, we check the conditions of Theorem 1. One could easily confirm that Theorem 1 is satisfied by the second condition, with the temperature CBF gain $K_T = 10^{-2}$, and

TABLE IV
PERFORMANCE METRICS.

Metric	Symbol	Formulation
Voltage derating	J_V	$\int_0^{t_f} \frac{ V_{DC} }{i_f V_{DC}^*} dt$
SoC balancing	J_{SoC}	$\int_0^{t_f} \sum_{k=1}^N Q_k(t) - \bar{Q}(t) dt$
Max. T violation	J_T	$\max_t (T(t) - T_{max}, 0)$
Avg. CPU time	J_{CPU}	$\int_0^{t_f} \frac{CPU_T(t)}{t_f} dt$
Energy loss	J_{EL}	$\int_0^{t_f} P_l(t) dt$

Notes: Avg.: Average;

$CPU_T(t)$ denotes CPU time for each optimization at time t ;

$\bar{Q}(t)$ denotes the average SoC of all battery modules at time t .

TABLE V
PERFORMANCE EVALUATION DEFINITIONS.

Control	J_V	J_{SoC}	J_T	J_{CPU}	J_{ELoss}
	-	-	$^{\circ}C$	ms	kJ
No Inner Control	1	144.0	1.40	12.7	3.73
MPC-H3*	1	96.7	0.20	33.9	2.98
MPC-H4	1	107.5	0.05	130.2	3.0
CA+CBF	1	60.4	0.00	21.1	2.79

* MPC-Hx refers to MPC with prediction horizon of x .

the parameters $\theta_1 = 10^{-3}$, $\overline{\Delta T}_k = T_{max} - T_a = 10^{\circ}C$, and choosing $\Delta T^* = 11^{\circ}C$. *Note*: the upper and lower bounds of this Theorem can be used as tuning guides for the CBF gains.

2) *SoC CBF*: computing an upper bound for the SoC balancing CBF gain depends on the maximum tolerable SoC imbalance, i.e. $\bar{\delta}_Q$. We assume that the initial variation of the battery SoC is no more than $\bar{\delta}_Q = 10\%$.

Based on Theorem 2, $\theta_{3,k} = 10^2 \frac{2}{C_{bat}} |i_{DC}|$ which is a function of the load current. Assuming a minimum load current of 1A, the upper bound value $\theta_{3,k} = 40.8$, which is the chosen value in our simulations and experimental results. Please note that with the increase of the load current, the upper bound for the SoC balancing constraint gain increases.

C. Control Performance Comparison

We compared the performance of the controlled battery system against the performance metrics defined in Table IV. These metrics assess the controllers with respect to average DC voltage derating (ideally 1 for no derating), overall SoC imbalances (as small as possible), maximum temperature violation (ideally 0), average CPU time and energy losses.

Table V presents the numerical results of the control strategies: 1) without inner control, 2) employing MPC with a prediction horizon of 3 and 4 seconds, and 3) utilizing CA+CBF. These results illustrate the significant superiority of CA+CBF over MPC, notably in CPU time, with an average speed improvement of 60.6% with respect to MPC with $H = 3$, and 51.7% faster than MPC with $H = 4$. Additionally, CA+CBF demonstrates better performance in SoC balancing,

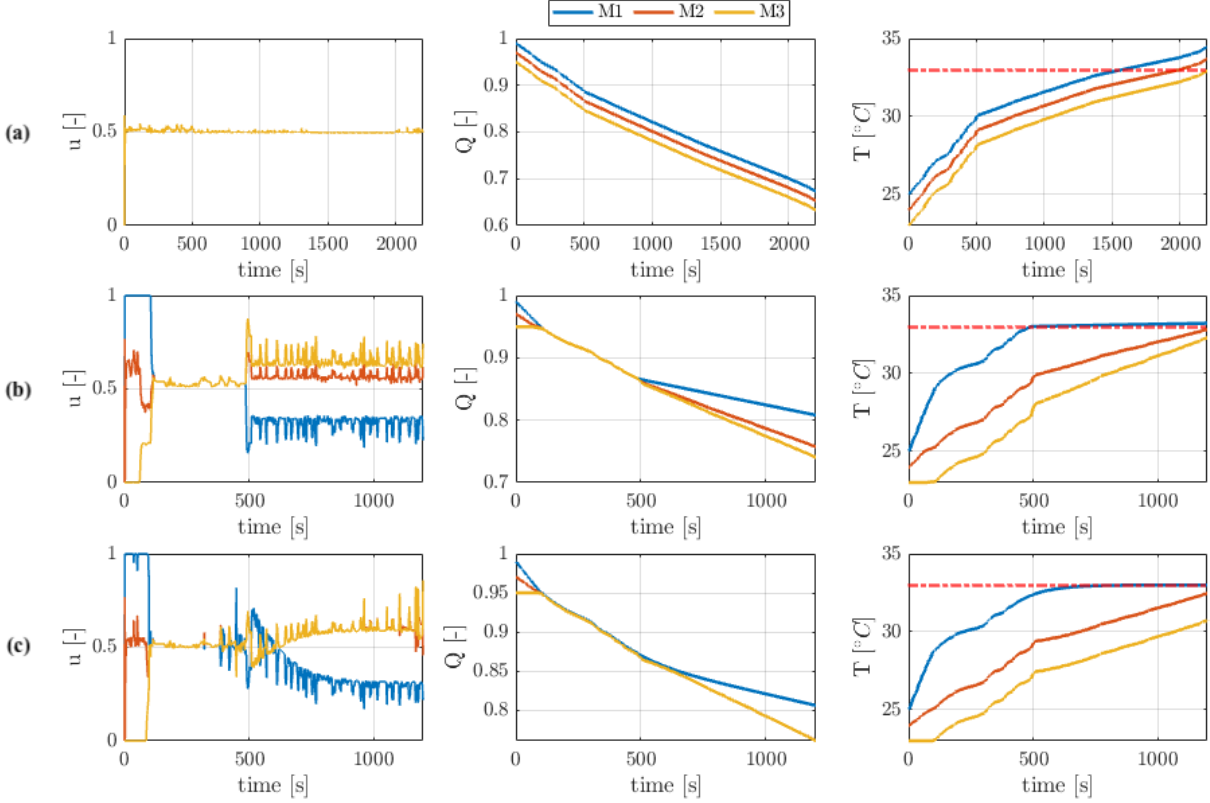


Fig. 9. Simulation results of the reconfigurable battery SoC balancing and temperature limit enforcement. **Top Row (a)**: No Inner Control. Equal discharging current from three modules. **Middle Row (b)**: MPC (with control horizon of 3 seconds) SoC balancing and temperature control simulation results; **Bottom Row (c)**: CA+CBF SoC balancing and temperature control simulation results.

exhibiting nearly a 59.6% difference compared to MPC with $H = 3$. Lastly, CA+CBF-based controller provides the lowest of the power losses among all controllers.

It is important to acknowledge the influence of the control horizon on MPC performance. While one might argue for the increased performance of MPC with a larger prediction horizon, this improvement comes at a computational cost. MPC with a horizon of 4 already requires 130.2 ms of CPU time on average when all constraints are active. This computational burden presents practical implications, which our CBF-based control approach addresses by achieving up to 6 times faster performance.

D. Module Scalability Analysis

In this section, we evaluate scalability of CA+CBF with increase in the number of battery modules. We increase the number of battery modules from $N = 4$ to $N = 8$, with one battery module increase at every iteration. With every module increase, we add one extra maximum temperature constraint, and N SoC balancing constraints to the CA+CBF. We assume batteries start with initial SoC that are randomly assigned from the range $[0.75, 1]$ and initial temperatures within $[T_{amb}, T_{amb}+3]$. Fig. 10 shows the series of simulation results of the cases where each row represents

$N = 4, 5, 6, 7, 8$, respectively. In addition, in these tests, we vary the battery capacities with $\pm 10\%$ variations from the nominal capacity $C_{nom} = 4.9\text{Ah}$. In all cases, we observe the effectiveness of the CBF constraints for SoC balancing $|Q_i - Q_j| \leq \Delta Q_{max}$, $i \neq j = 1, \dots, N$, and maximum temperature $T_{max} = 33^\circ\text{C}$. In the first row ($N = 4$), SoC balancing is achieved in less than 500s. During this period, the module with high SoC is discharged at the highest rate, leading to highest temperature in this module. After 800s, the duty cycle of the module with highest SoC is decreased in order to preserve temperature constraint (leading to SoC imbalance at the end of the driving cycle). For $N > 4$, we can observe a similar pattern: i) first phase where CA+CBF aims to balance SoC; ii) second phase where the overheating module(s) receive less load to preserve temperature limit. In the case with $N = 7$, due to the initialization values, all batteries are balanced while no module has reached the maximum allowed temperature.

1) *Effect of the Load Scaling Factor on the Average CPU Time*: in addition to the above results, Fig. 11 shows the effect of the load scaling factor on the averaged CPU time of each simulation. Load scaling factor ($\gamma_{load} \geq 1$) is a scalar

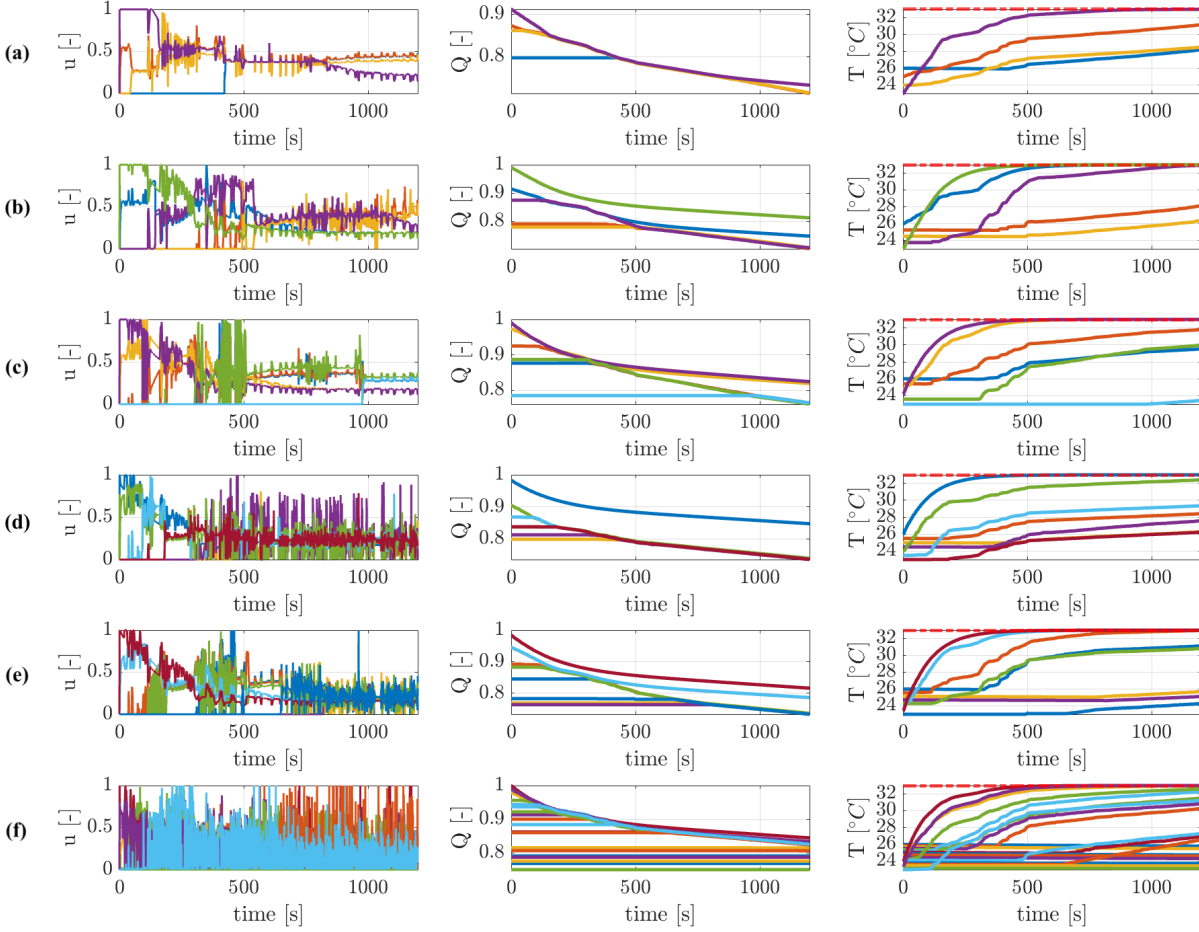


Fig. 10. Battery modules discharging under SoC balancing and temperature control. Each row (a)-(f) representing the control action, SoC evolution, and module temperatures for the cases $N = 4, 5, 6, 7, 8, 20$.

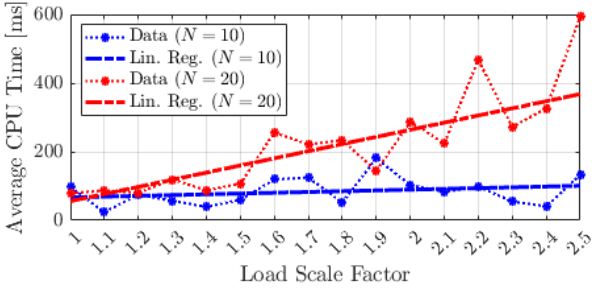


Fig. 11. Effect of the load scaling factor on the average CPU time of the RBs with $N = 10$ and $N = 20$ modules.

that is multiplied by the reference load power (P_{load}^*) profile²,

$$P_{load} = \gamma_{load} P_{load}^*$$

²For example on the FTP75 driving cycle profile represented in Fig. 8

Each simulation is initialized with random initial values for the SoC, temperature, and capacities for two cases of $N = 10$ and $N = 20$ modules, represented in blue and red, respectively. The bounds of the random initial values correspond to the values in Table III and the capacities are varied $\pm 5\%$ from the nominal value with a uniform distribution. Due to the probability distribution of the initial values, the average CPU time of each simulation in this figure is averaged for 3 tests. The results reveal an increasing trend of the average CPU time for either of the cases $N = 10, 20$. As more batteries approach T_{max} , more CBF constraints will be active, hence CPU time will increase. Furthermore, doubling the number of modules, results in an increased computational effort of the solver.

E. Impact of Numerical Solvers

Additionally, we also evaluate the impact of three different numerical solvers (fmincon, ipopt [57], and gurobi) in the

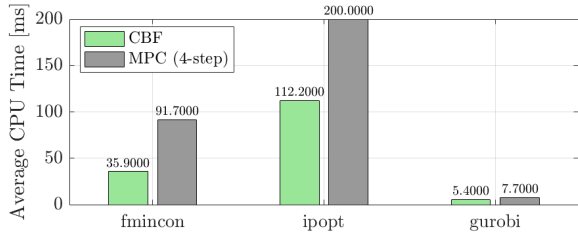


Fig. 12. Average computation time comparison of CBF and MPC (4-step horizon) controllers across three solvers: fmincon, ipopt, and gurobi. MPC is shown in gray and CBF in light green.

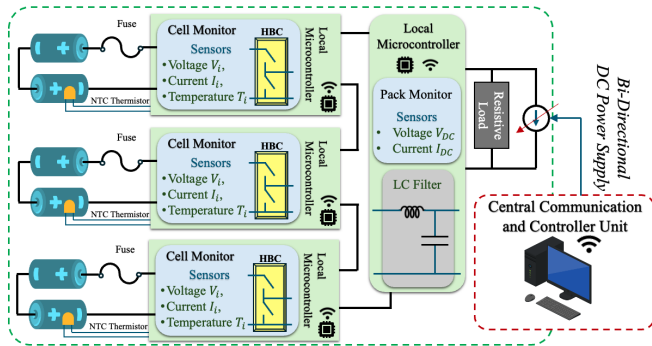


Fig. 13. Schematic representation of the experimental setup of the RB system.

computation time of the MPC and CA+CBF. From Fig. 12, we observe that “gurobi” is the fastest solver.

V. EXPERIMENTAL VALIDATION

A. Description of the Experimental Setup

The experimental prototype consists of three modules, each containing two batteries connected in series. The batteries used are SAMSUNG INR21700-50E Lithium-ion cells, with a standard discharge capacity of 4900 mAh. The modules are connected in series through half-bridge power converters, as shown in the schematics Fig. 1 and more detailed in Fig. 13. These converters facilitate balancing among the modules. We employed the MOTIX IFX007T half-bridge converter switches, which are controlled by PWM signals from an Arduino UNO R4 WiFi. Consequently, each battery module is connected to a Printed Circuit Board (PCB) that performs the following “cell” monitoring functions: 1) ACS723LLCTR-05AB-T hall effect current sensor, 2) module-level voltage measurement, 3) up to 4 individual cell voltage measurements, 4) $10k\Omega$ Negative Temperature Coefficient (NTC) thermistor (NXFT 15XH103FA2B130) for temperature measurement, and 5) half-bridge converter. Fig. 14 and Fig. 15 presents the experimental setup utilized for this validation.

An additional Arduino is used to perform “pack”-level measurements. This unit measures the pack’s voltage (using a voltage divider circuit) and current on the load side, after the LC filter. The Arduino in this unit and the battery modules communicate with the central communication and controller

TABLE VI
CONTROL PARAMETERS OF THE EXPERIMENTAL TESTS.

Parameter	Symbol	Test 1	Test 2
Power Loss Gain	ω_1	0	0
Voltage Slack	ω_2	10^5	10^5
SoC Slack	ω_3	2×10^4	10^5
Temp. Slack	ω_4	N/A	10^{12}
SoC CBF Gain	$K_{Q,k}$	0.5	0.5
Temp. CBF Gain	$K_{T,k}$	N/A	10^{-3}

unit (see Fig. 13) through WiFi, transmitting measured quantities and receiving duty cycle values from the computer. These values can be generated either manually by the user or computed by a controller. On the load side, we utilize an ITECH bi-directional DC Power Supply (IT-M3422) in parallel to a resistor to emulate the characterized load to the system (see Fig. 15).

To perform the module SoC balancing and temperature control, the CA+CBF requires the following states: 1) SoC (Q) and 2) temperature (T) of each module, 3) output voltage (V_{DC}), and 4) output current (i_{DC}). To estimate the SoC of each module, a coulomb counting approach is applied from the measured module current and the corresponding module’s duty cycle (direct application of equation (1a)). The remaining states we directly measure by temperature and current sensors.

B. Experimental Results

We experimentally validate CA+CBF with two test cases::

- SoC balancing with no temperature control for FTP75 driving cycle discharge power load;
- case above with temperature control.

Fig. 16 depicts the experimental results of the two controller variants. The controller parameters of these tests are summarized in Table VI. In the first test case (left column), the controller regulates the output voltage at 10V while distributing the duty cycles according to the load profile. The cell-to-cell SoC variations converge after approximately 200s and remain balanced throughout the driving cycle. However, without thermal constraints, all modules exceed the maximum allowable temperature, which highlights the need for thermal protection. The second test case (right column) addresses this limitation by enforcing the maximum temperature constraint in addition to SoC balancing. Similar to the first case, the SoC values are equalized within 200s. At this point, the first module reaches the temperature limit, and the controller reallocates the load by bypassing this module. As shown in the duty cycle response (blue line, $250s < t < 300s$), the first module is effectively disconnected while the remaining two modules supply the demand. This ensures thermal safety but comes at the expense of SoC balancing. This trade-off reflects the prioritization of temperature constraints over SoC balancing in the optimization cost function. As shown in TABLE VI, the slack variable

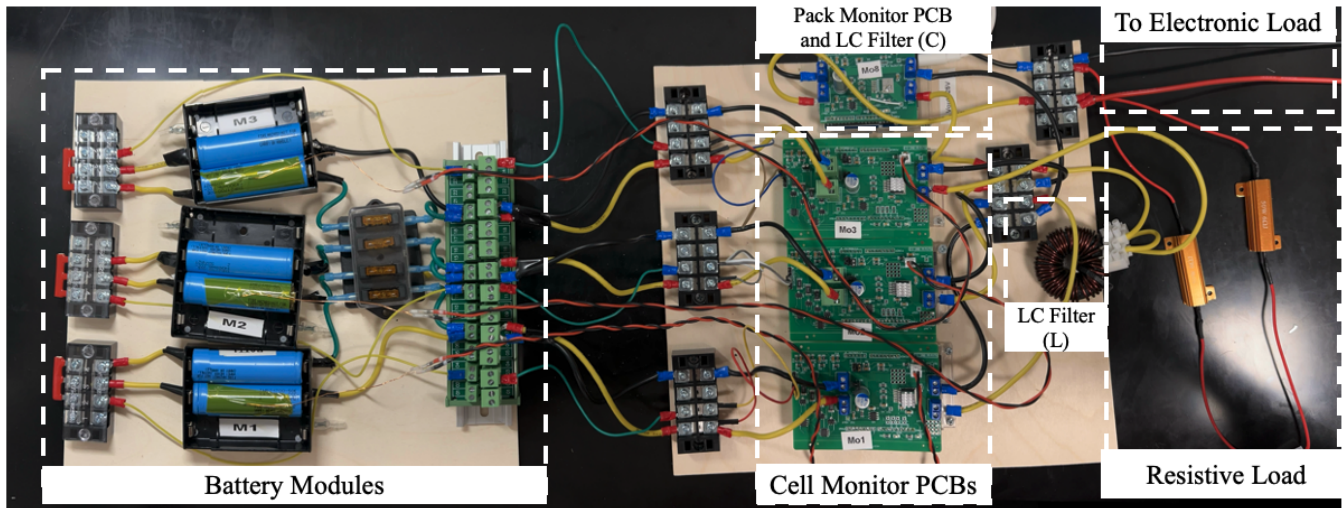


Fig. 14. Small-scale reconfigurable battery modules with balancing circuit experimental setup.

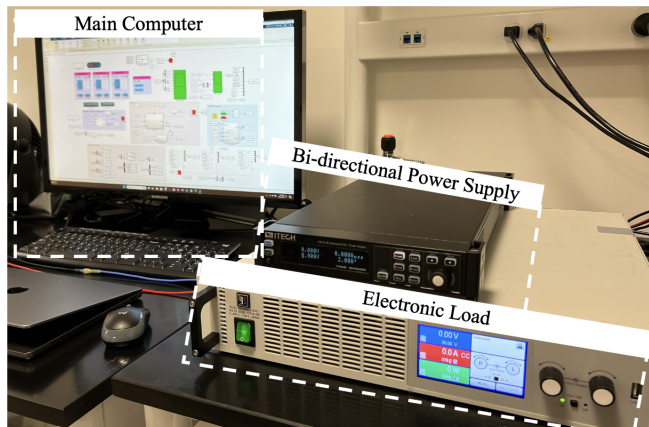


Fig. 15. Electronic Load: Bi-directional power supply to emulate the driving cycle or an electronic load for constant current loads. Main Computer: Main computing unit and controller implementation on MATLAB Simulink.

minimization gain for temperature is 10^7 times higher than that for SoC, leading the controller to favor thermal safety.

As shown in Fig. 17 and summarized in TABLE VII, the second test case, which includes thermal constraints, incurs a higher average CPU time than the first case (33.59ms vs. 29.38ms). Furthermore, Fig. 17 illustrates a noticeable increase in CPU time around $t = 100$ s, when the first module approaches the maximum temperature threshold. This rise corresponds to the controller's reconfiguration and reallocation process, which ensures safe operation by bypassing the overheated module. Additional performance metrics from TABLE VII highlight the trade-offs between the two cases. Both controllers achieve voltage regulation close to the reference value (voltage derating near unity). The second test case exhibits better thermal safety, reducing the maximum temperature violation from 8.93°C in the first test to only 0.54°C . However, this comes at the expense of state-of-charge balancing.

TABLE VII
EXPERIMENTAL PERFORMANCE EVALUATION.

Controller Variant	J_V	J_{SoC}	J_T	J_{CPU}
	-	-	$^\circ\text{C}$	ms
Without temperature control	0.996	274.53	8.93	29.38
With temperature control	0.969	548.19	0.54	33.59

VI. CONCLUSIONS

In this work, we introduced a novel control strategy combining CA and CBF to manage electro-thermal safety constraints in reconfigurable battery systems. Our approach offers significant computational advantages over MPC achieving comparable safety and performance results while operating at least 60% faster for a 3-second prediction horizon. A key contribution of this work is the feasibility analysis of the CA+CBF controller, including the derivation of CBF tuning gain that preserves numerical feasibility of the CA+CBF optimization problem for a wide range of operating conditions. Additionally, we also performed a scalability analysis of the CA+CBF with respect to the number of battery modules. We concluded that the computational effort is correlated with the mission profile. When high power is requested, more modules approach the thermal limits, making it increasingly difficult for the controller to efficiently find optimal solutions in short period of time. We experimentally validated the controller on a small-scale test bench. It safely discharges battery modules and maintains SoC balancing, provided the over-temperature protection is not violated.

Looking ahead, future research will focus on integrating the experimental setup with a battery management system capable of running real-time diagnostic algorithms. Such integration would enable continuous adaptation of key battery model parameters, including resistance and open-circuit voltage, thereby improving the accuracy of control decisions.

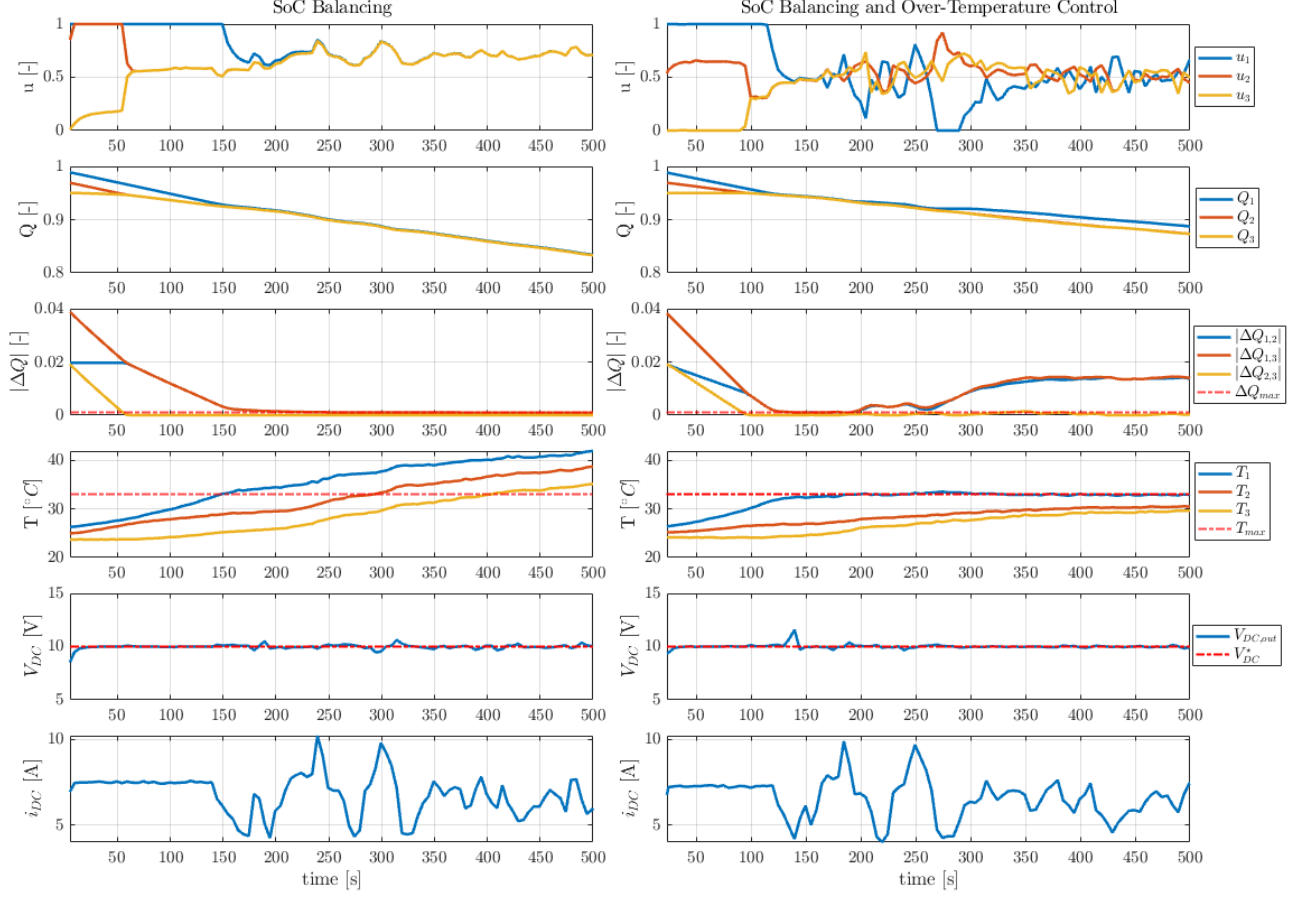


Fig. 16. Experimental results of CA+CBF: **Left column:** battery SoC balancing; **Right column:** and SoC balancing with maximum temperature control of the (properly scaled) FTP75 driving cycle discharging profile.

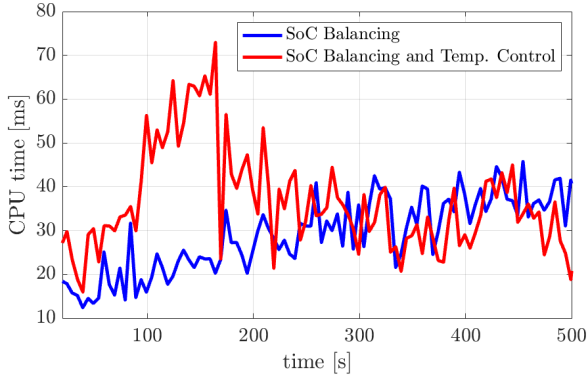


Fig. 17. CPU time comparison of the two experimental tests with CA+CBF.

Further enhancements to controller performance could be pursued through Bayesian optimization for systematic tuning of cost function weights. Finally, we plan to extend the CA+CBF framework by introducing a derating factor that

reduces the reference load power near thermal limits, and by incorporating liquid cooling actuator control to further enhance the thermal response of the battery thermal management system.

APPENDIX A MODEL PREDICTIVE CONTROL AS “BASELINE CONTROLLER”

Considering a prediction horizon of H , with sampling time of T_s , we formulate the following MPC-based optimization

problem,

$$\underset{\mathbf{u}[k]}{\text{minimize}} \quad \mathcal{J}_{\text{CA+MPC}}(\mathbf{u}[k]) \quad (36a)$$

subject to

$$\mathbf{u}[k] \in U = [0, 1]^N, \quad (36b)$$

$$V_N = V_{ref} + \delta_V[k], \quad (36c)$$

$$\mathbf{Q}[k+1] = \mathbf{Q}[k] + T_s (-\mathbf{C}_{\text{bat}}^{-1} i_{DC} \mathbf{u}[k]), \quad (36d)$$

$$\mathbf{T}[k+1] = \mathbf{T}[k] + T_s (\mathbf{f}_{\mathbf{T}}(\mathbf{T}[k], \mathbf{u}[k])), \quad (36e)$$

$$\mathbf{T}[k] \leq T_{max} \mathbf{1}_N + \mathbf{s}_{\mathbf{T}}[k], \quad (36f)$$

$$0 \leq \delta_V[k], \quad \mathbf{0}_N \leq \mathbf{s}_{\mathbf{T}}[k], \quad (36g)$$

$$k = 0, 1, \dots, H-1 \quad (\text{prediction horizon}),$$

where the system dynamics is discretized with the Forward Euler method, in (36d) and (36e). Moreover, the function in (36e) summarizes the thermal model:

$$\mathbf{f}_{\mathbf{T}}(\mathbf{T}[k], \mathbf{u}[k]) = -\mathbf{C}_{\mathbf{T}}^{-1} \mathbf{R}_{\mathbf{C}}^{-1} (\mathbf{T}[k] - \mathbf{T}_{\mathbf{a}}) + \mathbf{C}_{\mathbf{T}}^{-1} \mathbf{u}^{\top}[k] \text{diag}(\mathbf{R}_{\mathbf{b}}) i_{DC}^2 \mathbf{u}[k]. \quad (37)$$

Lastly, the cost function $\mathcal{J}_{\text{CA+MPC}}(\mathbf{u}[k])$ encodes

$$\begin{aligned} \gamma_1 \sum_{k=0}^{H-1} \delta_V[k]^2 + \gamma_2 \sum_{k=0}^{H-1} \sum_{j=1}^N (Q_j[k] - \bar{Q}[k])^2 + \\ + \gamma_3 \sum_{k=0}^{H-1} \|\mathbf{s}_{\mathbf{T}}[k]\|^2 + \gamma_4 \sum_{k=0}^{H-1} \|\mathbf{u}[k]\|^2, \end{aligned} \quad (38)$$

which is aimed to minimize reference voltage derating, module-to-module SoC variations, temperature slack variable, and control effort in respective order. Furthermore, $\gamma_i, i = \{1, 2, 3, 4\}$ are the control tuning gains.

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